ANNOUNCEMENT

Workshop on ASIC Design & CMOS Process Technologies

24th May -26th May, 2011

National Centre for Physics, Islamabad

The Experimental High Energy Physics Group of National Centre for Physics (NCP) is organizing a workshop on ASIC Design and CMOS Process Technologies in collaboration with Advanced Electronics Laboratory, Faculty of engineering & technology, International Islamic University Islamabad (IIUI). The main objective of this workshop is to prepare a group of trained young Engineers/Scientist who can develop a new ASIC design as per requirement and learn about Nano-meter (nm) design challenges. This will provide them with an opportunity to carry out research in the fields of VLSI/ULSI design and fabrication. A Lab session will also be conducted to provide hands-on training on SILVCO-TCAD. The hands-on series will be carried out in IIU's Advance Electronics Design Suits. At the end of the workshop, certificates will be awarded to the participants.

Participants

A total of 50 participants will be invited from all over the country to attend this workshop. Process integration Engineers & Scientists, Device Physicists/Engineers, VLSI/ULSI researchers, Nanotechnologists and Electronic Engineers are encouraged to apply.

Topics to be Covered

1-1 Semi- Conductor device manufacturing technologies, CMOS, Strong '1' & Strong '0', GaAs HIgh speed digital logic families

1-2 Full / Semi custom ASICs, CBICs, MGAs and FPGAs, basic cell structure, Cell libraries primitives, push-pull techniques

1-3 Internal Structures of FPGAs, ASIC / FPGA comarison: Design limitations, constraints and net lists. Mixed signals ICs

2-1 Back End of line processing, short channel effects

2-2 Manufacturing issues, critical dimension and ultra shallow junction issue. What is Next in desing challenges?

2-3 Lab (Silvaco - TCAD) on an industrial trade off desing tool

3-1 Introduction to Integrated Circuits, Latest Trends in Integrated Circuit Design, CMOS tech and design kit, Design Methodology and CAD tools, Preamplifer Example, System Modeling and Parameters Extraction, Circuit Design-Gain, Noise, input, impedance and output impedance calculations, Layout and Post Layout Simulation, Tape out and Measurements

3-2 Introduction, HBTs and Analgue to digital converters, HBTs physical device modelling in SILVACO, MMICs Fabrication, Parametrical Modelling and Device Characterization, Low Power, High speed Digital Circuits and ADCs, InAlAs / InGaAs Ternary HBTs, Conclusion and Further work

Master Trainers/Speakers:

1. Dr. Ahmad Shuja Syed (IIUI)
2. Dr. Yousuf Zafar (ICCC)
3. Dr. Tauseef Tauqeer (NUST)
4. Abdullah Mansoor (NUST)
5. Shoaib Ahmed (IIUI)
6. Syed Mashhod Murtaza (IIU)

Contact Person:

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Registration Fee

Students: 1000/-
Professionals: 2000/-

Registration Form Available at NCP website: www.ncp.edu.pk/sslp.htm

Registration Deadline

10 May, 2011

For any further information please contact

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